Shruti Patil

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Research Interests

Next-generation Computing; Circuits, Architectures and Systems with Emerging Technologies (Spintronics, Quantum Computing, NEMS, etc.); Unconventional computer architectures; Mobile Computing.

Professional Preparation

Mar'14–May'15 **University of California San Diego** . . . . . San Diego, CA
Postdoctoral Scholar
Power and performance optimizations on mobile platforms using non-volatile memories and user-behavior awareness

Mar'13–Mar'14 **Princeton University** . . . . . Princeton, NJ
Postdoctoral Research Associate
Compiler framework for quantum programs; analysis and optimization techniques for large-scale quantum programs; design of parallel quantum architectures.

2006–2011 **University of Minnesota** . . . . . Minneapolis, MN
Ph.D. Electrical Engineering
Dissertation: Development of Next-Generation Computing Elements Fabricated Using Emerging Technologies (Spintronics and CarbonNanoTube-based NEMS)
Advisor: Prof. David J. Lilja

2004–2006 **University of Nevada Las Vegas** . . . . . Las Vegas, NV
M.S. Electrical Engineering
Thesis: Maximizing Resource Utilization by Slicing of Superscalar Architectures
Advisor: Prof. Venkatesan Muthukumar

2000–2004 **University of Mumbai – VJTI** . . . . . Mumbai, India
Bachelor of Engineering, Computer Engineering
First Class with Distinction

Industry Experience

May'15–present **Software Engineer at Google Inc.** . . . . . Mountain View, CA
Ads Quality Team
Performance Modeling and Statistical Analysis

Jan'12–Mar'13 **Research Scientist at Intel** . . . . . Santa Clara, CA
Microarchitectural Research Lab (MRL)
Performance modeling, Statistical techniques for Design Exploration, Simulation framework for mobile application characterization

Aug'11–Dec'11 **Graduate Technical Intern at Intel** . . . . . Santa Clara, CA
Microarchitectural Research Lab (MRL)
Performance modeling and analysis of microarchitectures.

May'08–Aug'08 **Graduate Technical Intern at Intel** . . . . . Folsom, CA
Architectural Research and Evaluation Team
Modeling and evaluation of microarchitectures on Massively Parallel Architecture Array for accelerated hardware emulation.

May'07–Aug'07 **Graduate Technical Intern at Intel** . . . . . Folsom, CA
Simulation Acceleration Team
Algorithms for partitioning and mapping microarchitectural designs on FPGAs.

Patent

US 8634233 B2 *Systems and Methods for Direct Communication between Magnetic Tunnel Junctions*
University of Minnesota
Circuit design and fabrication methodology for a fully-spintronic, programmable logic on spintronic data directly without intermediate CMOS conversion circuitry.

Publications

Mobile and Low Power Computing Systems

[C20] M. Imani, **S. Patil**, T. Rosing, *"MASC: Ultra-Low Energy Multiple-Access Single-Charge TCAM for Approximate Computing"*, To be presented at IEEE Conference on Design, Automation and Test in Europe (D.A.T.E), March 2016.

[C19] M. Imani, **S. Patil**, T. Rosing, *"Low Power Data-Aware STT-RAM based Hybrid Cache Architecture"*, To be presented at 17th International Symposium on Quality Electronic Design (ISQED), March 2016.

[C18] **Shruti Patil**, Yeseong Kim, Kunal Korgaonkar and Ibrahim Awwal, "Characterization of User's Behavior Variations for Design of Replayable Mobile Workloads", International Conference on Mobile Computing, Applications, and Services (MobiCASE 2015), Nov 12-15, Berlin, Germany, 2015.

[C17] **Shruti Patil**, Yu Chen and T. Rosing, *"GazeTube: Gaze-Based Adaptive Video Playback for Bandwidth and Power Optimizations"*, IEEE Globecom, Dec 2015.

[C16] Yeseong Kim, Mohsen Imani, **Shruti Patil** and T. Rosing, *"CAUSE: A critical application usage-aware memory architecture using non-volatile memory for mobile devices"*, Accepted at IEEE/ACM 2015 International Conference On Computer Aided Design (ICCAD), Nov 2-6 2015, Austin, TX.

[C15] Mohsen Imani, **Shruti Patil** and T. Rosing, *"Hierarchical Design of Robust and Low Data Dependent 32kB FinFET-based SRAM Array"*, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), July 8-10, 2015, Boston, US.

[Poster2] Mohsen Imani, **Shruti Patil** and T. Rosing, *"Ultra-Low Read Leakage SRAM Cell Utilizing Independently-Controlled-Gate FinFETs"*, Work-In-Progress Poster Session, Design Automation Conference (DAC), June 2015.

Quantum Computing - Compiler, Program Analysis and Architectures

[C14] J. Heckey, **S. Patil**, A. Javadi-Abhari, A. Holmes, D. Kudrow, K. Brown, D. Franklin, M. Martonosi and F. Chong, *"Compiler Management of Communication and Parallelism for Quantum Computation"*, ASPLOS, March 2015 (Acceptance rate 17.26%).

[C13] **S. Patil**, A. Javadi-Abhari, C. Chiang, J. Heckey, M. Martonosi and F. Chong, *"Characterizing the Performance Effect of Trials and Rotations in Applications that use Quantum Phase Estimation"*, IEEE International Symposium on Workload Characterization (IISWC), Oct 2014 (Acceptance rate 27.5%).

[J7] A. Javadi-Abhari, **S. Patil**, D. Kudrow, J. Heckey, A. Lvov, F. Chong and M. Martonosi, *"ScaffCC: Scalable compilation and analysis of quantum programs"*, ACM Parallel Computing, 2014.

[C12] A. Javadi-Abhari, **S. Patil**, D. Kudrow, J. Heckey, A. Lvov, F. Chong and M. Martonosi, *"ScaffCC: A Framework for Compilation and Analysis of Quantum Computing Programs"*, ACM Computing Frontiers 2014, Italy, 2014. **BEST PAPER AWARD**

Computer Performance Measurement - Statistical Analysis

[J6] **S. Patil** and D. Lilja, *"Statistical Methods for Computer Performance Evaluation"*, Wiley Interdisciplinary Reviews, April 2011.

[J5] **S. Patil** and D. Lilja, *"Using Resampling Techniques to Compute Confidence Intervals for the Harmonic Mean of Rate-Based Performance Metrics"*, IEEE Computer Architecture Letters, IEEE Computer Society, Jan. 2010.

Spintronics - Non-Volatile Computing Circuits

[Poster1] M. Imani and **Shruti Patil**, "Using STT-RAM Based Buffers in Digital Circuits", Poster, Non-Volatile Memories Workshop, March 2015.

[C11] **S. Patil** and D. Lilja, *"Performing Bitwise Logic Operations In Cache Using Spintronics-Based Magnetic Tunnel Junctions"*, ACM Computing Frontiers 2011, May 2011.

[C10] **S. Patil** and D. Lilja, *"A Programmable and Scalable Technique To Design Spintronic Logic Circuits Based On Magnetic Tunnel Junctions"*, ACM Great Lakes Symposium on VLSI (GLSVLSI '11), May 2011.

[J4] A. Lyle, **S. Patil**, J. Harms, B. Glass, X. Yao, D. J. Lilja, and J.-P. Wang,*"Magnetic Tunnel Junction Logic Architecture for Realization of Simultaneous Computation and Communication"*, IEEE International Magnetics Conference (InterMag), April 2011. IEEE Transactions on Magnetics, vol.47, no.10, pp.2970-2973, Oct. 2011.

[Talk] **S. Patil** and D. Lilja, *"Spintronics-Based Logic Circuits Using Magnetic Tunnel Junctions"*, Talk at 2nd Annual Non-Volatile Memories Workshop, San Diego, CA, March 2011.

[C9] **S. Patil**, A. Lyle, J. Harms, D. Lilja and J.-P. Wang, *"Spintronic Logic Gates for Spintronic Data Using Magnetic Tunnel Junctions"*. International Conference on Computer Design (ICCD), Amsterdam, Netherlands, Oct 2010.

[J3] A. Lyle, J. Harms, **S. Patil**, D. Lilja and J.-P. Wang, *"Direct Communication Between Magnetic Tunnel Junctions for Non-Volatile Logic Fan-Out Architecture*, Applied Physics Letters, Sept 2010.

[C8] **S. Patil**, X. Yao, H. Meng, J.-P. Wang, D. Lilja, *"Design of a Spintronic Arithmetic and Logic Unit Using Magnetic Tunnel Junctions"*, ACM Computing Frontiers 2008, Ischia, Italy, May 5-7, 2008, pp. 171-178.

Nano-Electro-Mechanical Systems (NEMS) - Logic Design

[C7] **S. Patil**, M-W. Jang, C-L. Chen, D. Lee, Z. Ye, W. Partlo III, D. Lilja, S. Campbell, T. Cui, *"Weighted Area Technique for Electromechanically enabled Logic Computation with Cantilever-Based NEMS Switches"*, Design, Automation and Test in Europe (D.A.T.E.), March 2012.

[C6] M-W. Jang, C-L. Chen, W. Partlo III, **S Patil**, D. Lee, Z. Ye, D. Lilja, T. Taton, T. Cui and S. Campbell, *"A Three-terminal Single-walled Carbon Nanotube Thin Film MEMS Switch for Digital Logic Applications,"* International Conference on Solid-State Sensors, Actuators, and Microsystems (TRANSDUCERS), June, 2011.

[J2] M-W. Jang, C-L. Chen, W. Partlo III, **S. Patil**, D. Lee, Z. Ye, D. Lilja, T. Taton, T. Cui and S. Campbell, *"A Pure Single-Walled Carbon Nanotube Thin Film Based 3-Terminal MEMS Switch"*, Applied Physics Letters, Vol. 98, No. 7, Jan. 2011.

During Master's Program - Computer Architecture, Reconfigurable Logic, Logic Synthesis, Wireless Sensor Networks, Neutron Detector Physics

[C5] **S. Patil** and V. Muthukumar,*"Maximizing Resource Utilization by Slicing of Superscalar Architecture"*, 11th Euromicro Conference on Digital System Design (DSD), Parma, Italy, Sept.3-5, 2008.

[J1] D. Rao, **S. Patil**, N. Anne and V. Muthukumar, *"Implementation and Evaluation of Image Processing Algorithms on Reconfigurable Architecture using C-based Hardware Descriptive Languages"*, Intl. Journal of Theoretical and Applied Computer Sciences, Vol. 1, 2006.

[C4] A. Raina, **S. Patil**, V. Muthukumar, A. Abraham, *"HAUNT-24: Hierarchical, Application Confined Unique Naming Technique"*, IEEE Conference Proceedings of Fifth International Conference on Intelligent Systems Design and Applications (ISDA 2005).

[C3] **S. Patil**, V. Muthukumar , *"Simultaneous Column Minimization-Encoding approach for Serial Decomposition"*, IEEE Proceedings of International Conference on Computational Intelligence and Multimedia Applications Conference (ICCIMA), August 2005, Las Vegas, NV, USA.

[C2] **S. Patil**, N. Anne, U. Thirunavukkarasu, E. Regentova, *"Branch Prediction by Checking Loop Terminal Conditions"*, Information Systems: New Generations (ISNG) Conference Proceedings, April 2005, Las Vegas, NV, USA.

[C1] **S. Patil**, T. Beller, B. Howard, D. Beller, *"Neutron Detector Characteristics in Dead Time Experiments"*, American Nuclear Society Student Conference, April 15, 2005. **Awarded Second Best Student Presentation.**

Teaching

Spring'10	*EE 8950 Teaching Experience in EE, University of Minnesota*
Fall '09	*GRAD 8101 Teaching in Higher Secondary Education, Preparing Future Faculty*
Sep'06-Dec'10	*Teaching Assistant at University of Minnesota* Computer Systems Performance Evaluation, Logic Design, Intro. to Microcontrollers
Sep'05-May'06	*Teaching Assistant at University of Nevada Las Vegas* Digital Logic Design, Computer Communication Networks, Digital Electronics, Computer Electronics Laboratory.

Honors and Awards

2014	Best Paper Award - ACM Computing Frontiers 2014, Peer-reviewed Conference, Italy
2014	Selected for *'2014 Rising Stars in EECS'* workshop, UC Berkeley
2014	Selected to participate in 'Prospective Faculty Workshop' at Purdue University
Aug'11	James Zeese Fellowship Award for PhD Dissertation, Dept. of ECE, U. of Minnesota
1998	National Talent Search Scholarship, India
1998	Ranked 6 at Regional Mathematics Olympiad, Mumbai, India
1997	Bombay Talent Search Award, Mumbai, India

Academic Service

2014 and 2015	Program Committee Member, Non-Volatile Memories Workshop (NVMW), San Diego (2yrs on the committee)
Jun'10-May'12	Member, Senate Committee of Finance and Planning, Univ. of Minnesota
Sep'10-May'11	Women's Graduate Group in EE Co-ordinator, Univ. of Minnesota
Jun'08-May'10	Member, Senate Committee of Student Behavior, Univ. of Minnesota
Jun'07-May'08	Member, Senate Library Committee, Univ. of Minnesota
Jun'03-May'04	General Secretary, Student's Council, VJTI, Univ. of Mumbai, INDIA

Reviewer

Journal - Parallel Computing (Parco), 2015
Workshop - Non-Volatile Memories Workshop (NVMW), 2014 and 2015.
Journal - Transactions on Architecture and Code Optimization (TACO), 2014
Journal - IEEE Transactions on Circuits and Systems-Part I (TCAS-I), 2013
Conference - International Symposium on Computer Architecture (ISCA), 2013
Conference - International Conference on Parallel Computing Technologies (PACT), 2012